

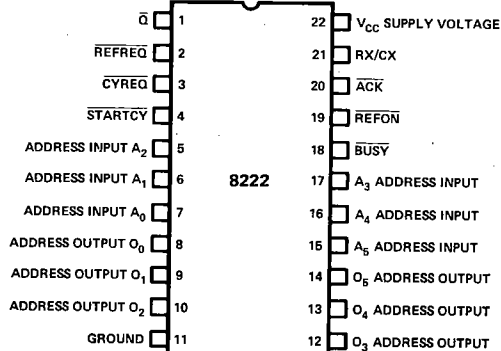
DYNAMIC MEMORY REFRESH CONTROLLER

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

- Adjustable Refresh Request Oscillator
- Ideal for 8107A, 8107B 4K RAM Refresh
- Internal Address Multiplexer
- Up to 6 Row Input Addresses (64 x 64 Organization)

The 8222 is a refresh controller for dynamic RAMs requiring row refresh of up to 6 row input addresses (or 4K bits for 64 x 64 organization). The device contains an accurate refresh timer (whose frequency can be set by an external resistor and capacitor) plus all necessary control and I/O circuitry to provide for the refresh requirements of dynamic RAMs. The chip's high performance makes it especially suitable for use with high speed N-channel RAMs like the 8107B. The 8222 is designed for large, asynchronously driven, dynamic memory systems.

PIN CONFIGURATION



BLOCK DIAGRAM

